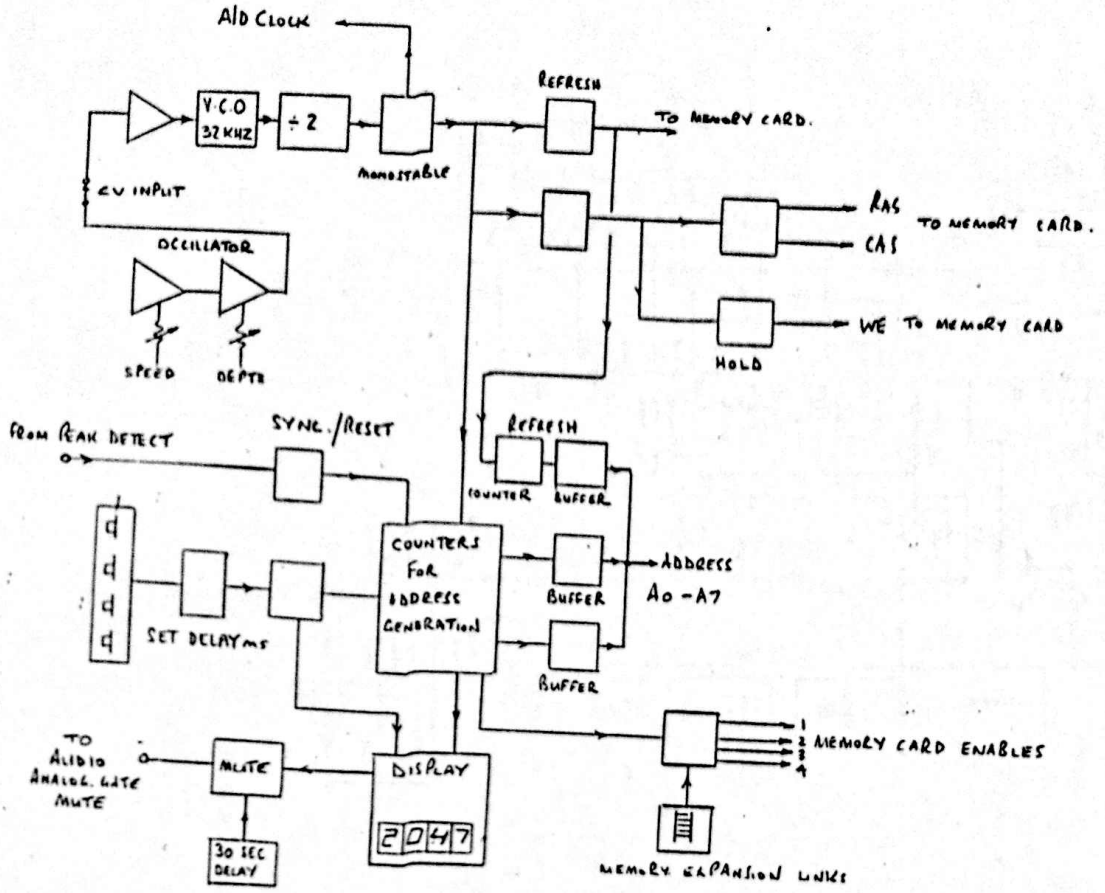
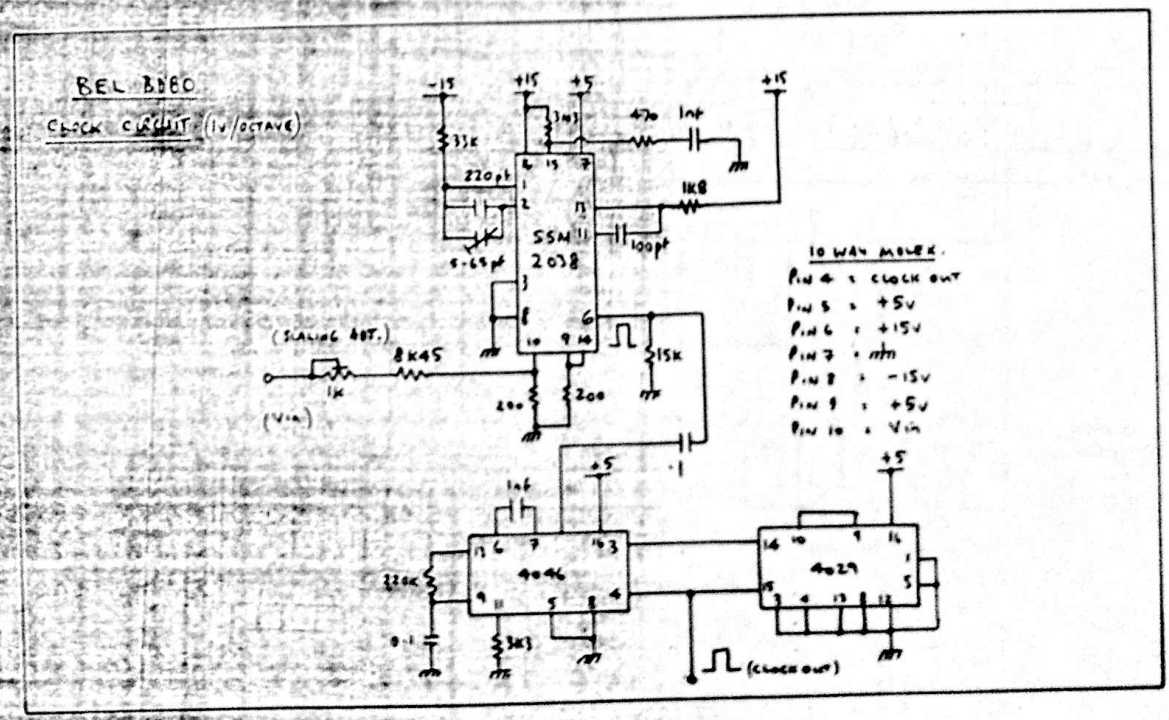
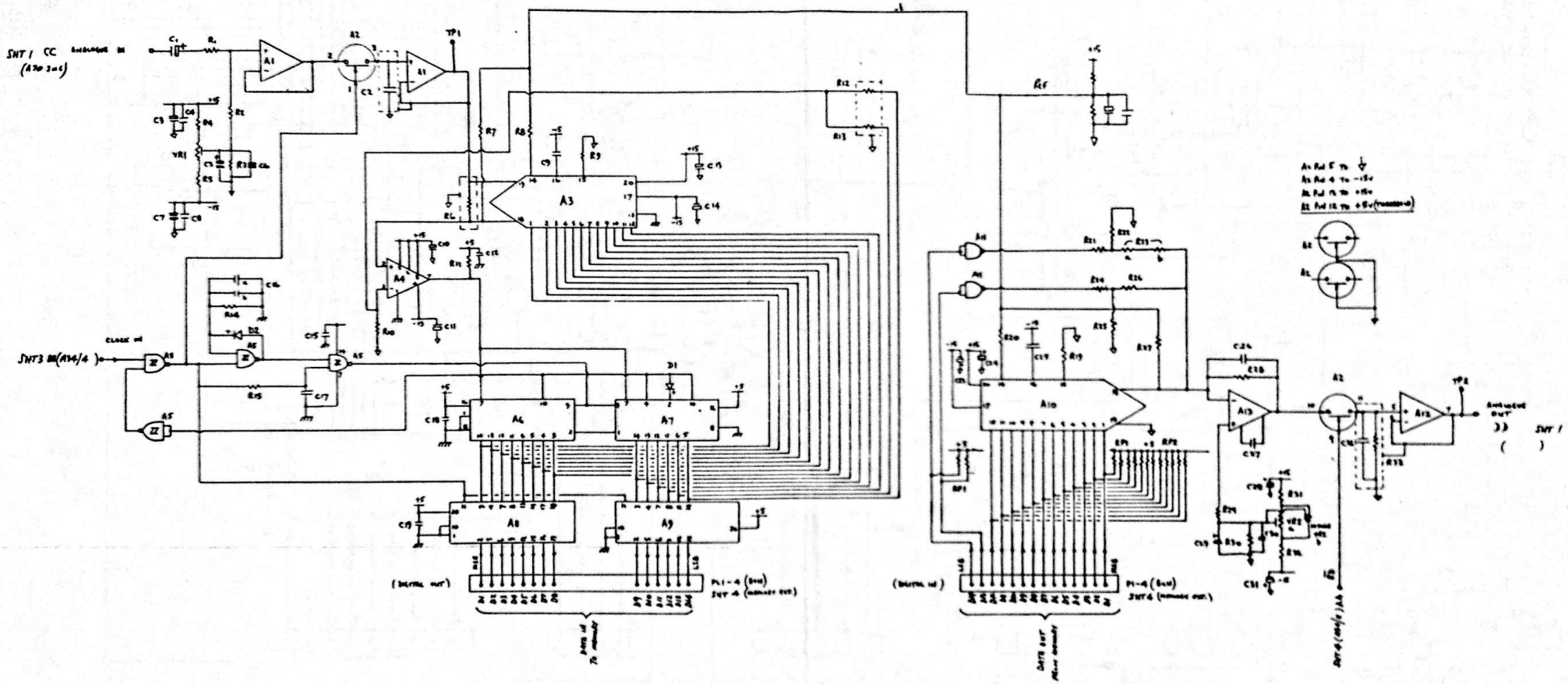
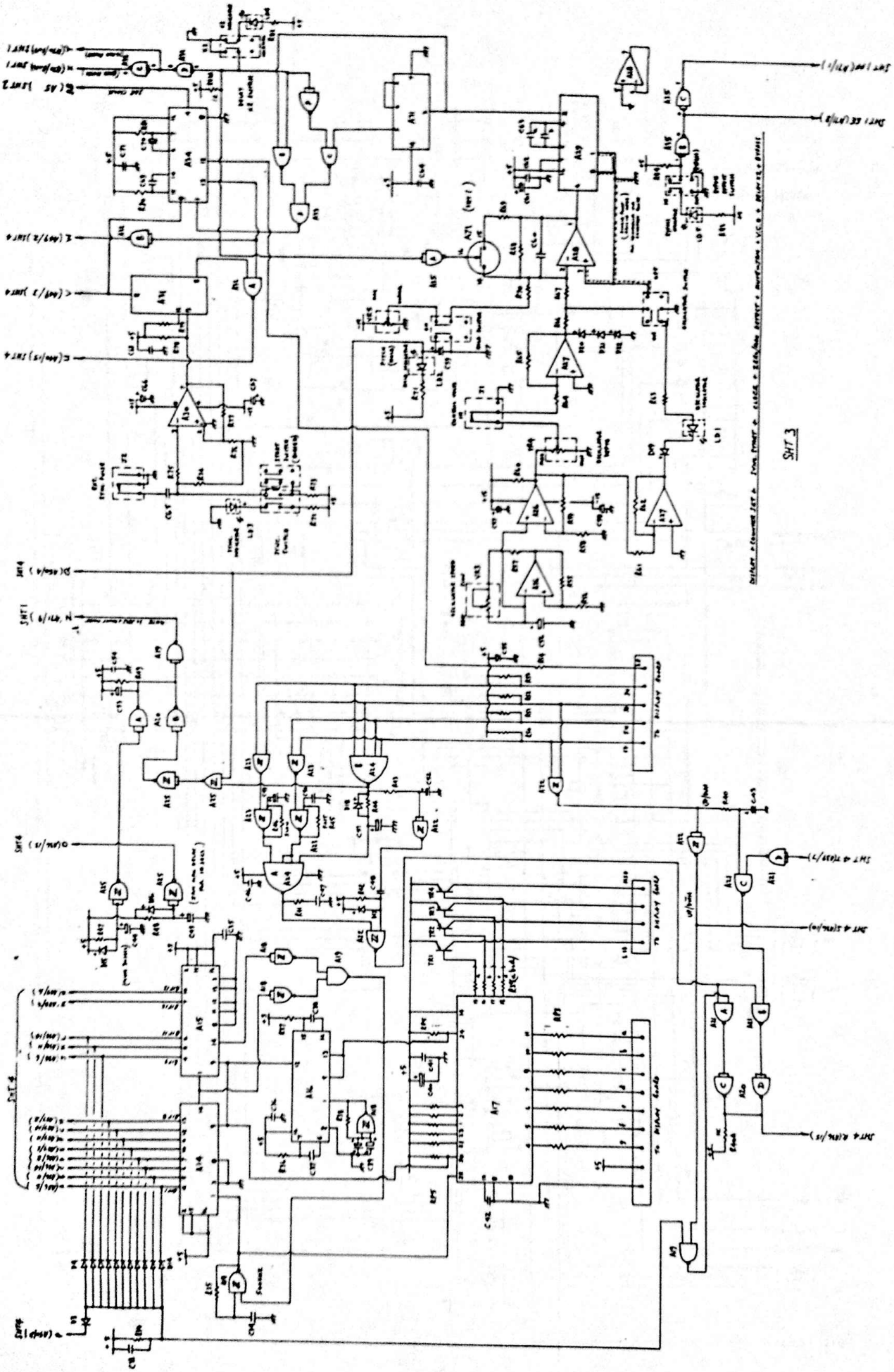
DIGITAL SIGNALS

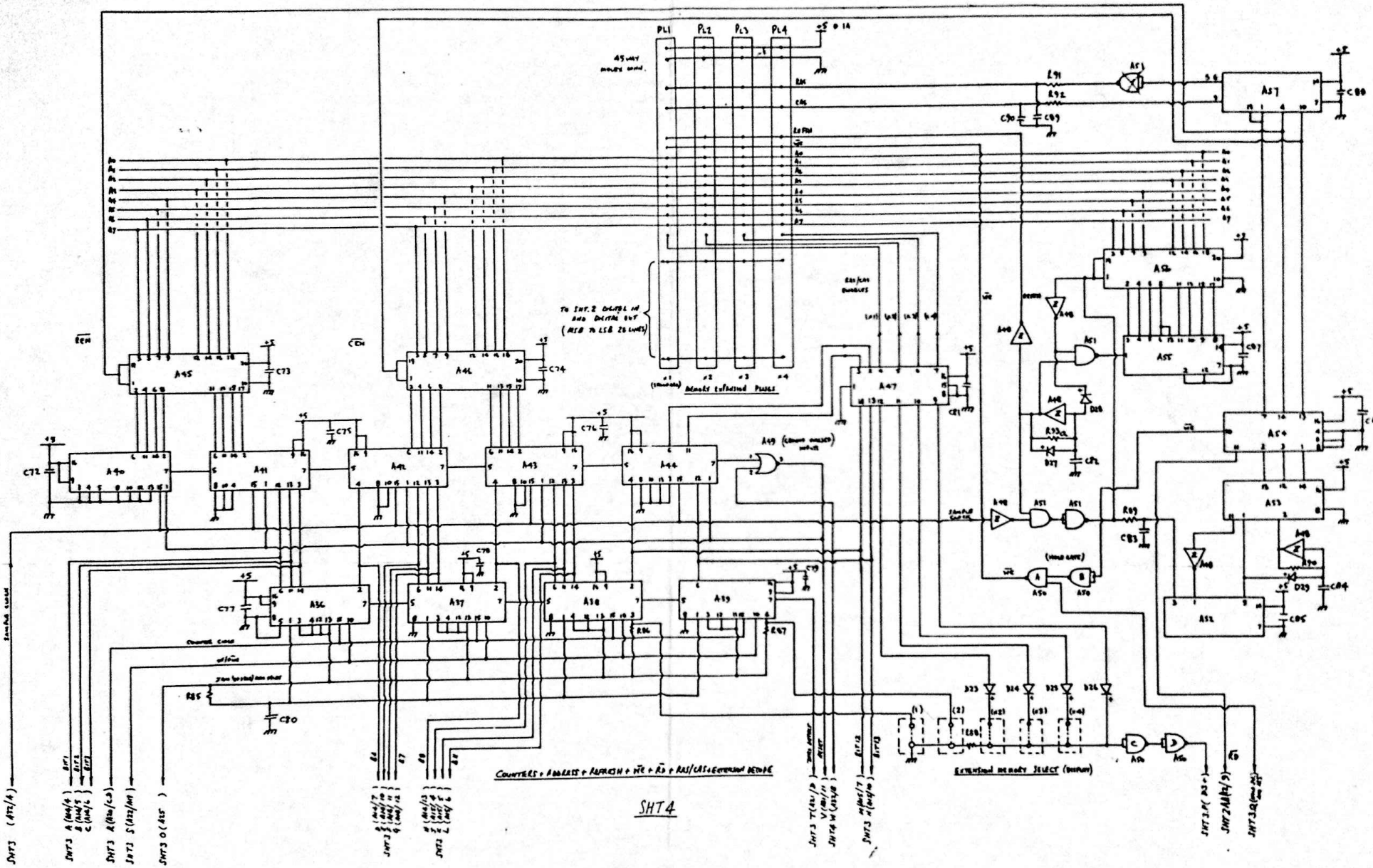
DIAGRAM 2






SHT 2
DIGITAL TO ANALOGUE AND ANALOGUE TO DIGITAL CONVERTERS




PL1
PL2
PL3
PL4
45 WAY MEMORY BUS.
MEMORY EXPANSION PLUGS
To INT. 2 DIGITAL IN AND DIGITAL OUT (MSB TO LSB 26 LINES)
A40
A41
A42
A43
A44
A45
A46
A47
A48
A49 (REFRESH ENABLED) INPUT
A50
A51
A52
A53
A54
A55
A56
A57
A58
A59
R91
R92
R93
R94
R95
R96
R97
R98
R99
C70
C71
C72
C73
C74
C75
C76
C77
C78
C79
C80
C81
C82
C83
C84
C85
C86
C87
C88
C89
D23
D24
D25
D26
D27
D28
D29
SAMPLE START
COUNTER CLOCK
WRITE
ZERO CROSSING ENABLE
SAMPLE CLOCK
(READ GATE)
COUNTERS + ADDRESS + REFRESH + WE + RD + RAS/CAS + EXPANSION BUSSES
EXPANSION MEMORY SELECT (DECODE)
SHT4